REMARKS

This application has been carefully reviewed in light of the Office Action dated August 24, 2006. Claims 1 to 7 are pending in the application, of which Claim 1 is the sole independent claim. Reconsideration and further examination are respectfully requested.

Claim 1 was rejected under 35 U.S.C. § 112, first paragraph, for allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Claims 1 to 3, 5 and 6 were rejected under 35 U.S.C. § 103(e) over U.S. Patent No. 6,124,888 (Terada). Reconsideration and withdrawal of these rejections are respectfully requested.

The present invention concerns an image processing apparatus havinga sensor which includes a plurality of pixels each including at least a light receiving element (for example, a photodiode), an amplifier element (for example, an amplifier transistor) and a selecting element (for example, a selecting transistor), wherein electrical signal from said light receiving element is output to a common output line through the selecting element, and is arranged to supply a first pulse to the selecting element of a pixel to be read out, when a first resolution is selected, and supply the first pulse to the selecting element of the pixel to be read out and a second pulse smaller than the first pulse to the selecting element of the pixel to be thinned out, when a second resolution lower than the first resolution is selected.

Turning to specific claim language, amended independent Claim 1 is directed to an image processing apparatus which includes a sensor including a plurality of

pixels each including at least a light receiving element, an amplifier element and a selecting element, wherein an electrical signal from the light receiving element is output to a common output line through the selecting element; a scanning circuit for reading out the electrical signal in time sequence from the plural pixels; and a drive circuit which supplies pulses to the selecting element. The drive circuit is so arranged to drive the scanning circuit so that the scanning circuit supplies a first pulse to the selecting element of a pixel to be read out, when a first resolution is selected, and supplies the first pulse to the selecting element of the pixel to be read out and a second pulse smaller than the first pulse to the selecting element of a pixel to be thinned out, when a second resolution lower than the first resolution is selected.

Applicant respectfully submits that Terada fails to disclose or suggest an image processing apparatus having at least the features of an amplifier element and a selecting element, wherein an electrical signal from a light receiving element is output to a common output line through said selecting element; a scanning circuit for reading out the electrical signal in time sequence from the plural pixels; and a drive circuit so arranged to drive said scanning circuit so that said scanning circuit supplies a first pulse to said selecting element of a pixel to be read out, when a first resolution is selected, and supplies the first pulse to said selecting element of the pixel to be read out and a second pulse smaller than the first pulse to said selecting element of a pixel to be thinned out, when a second resolution lower than the first resolution is selected.

Terada discloses an image pickup apparatus which reads out image information with thinning-out (skipping) of horizontal lines, as shown in Fig. 26. Specifically, Terada controls selection and non-selection (skip) of the horizontal line using

combination of pulses FV1 andFSRn, supplied during a horizontal blanking (HBL) period. In this connection, the Office Action refers to Figs.2F and 2G, for example, to content that Terada discloses long and short pluses. However, those figures show that in interlace scanning, a high level signal is supplied during one horizontal period to a level mixing circuit 13 to read out a line to be read, and a low level signal is supplied also to the level mixing circuit 13 to skip a line to be skipped. In addition, in Fig.2G, a short pulse supplied to skip a line is supplied in the HBL period which is not a signal reading period, and therefore, in the interlace scanning, no signal is read out from the skipped line.

However, it cannot be fairly said that this structure of Terada discloses or suggests the features of the present invention as recited in the amended independent Claim 1, since Terada is silent on supplying the long and short pluses to respective selecting transistors of pixels of a sensor. In contrast, amended independent Claim 1 clearly recites that each of two pulses of different widths are supplied to a selecting transistor of a pixel. That is, the apparatus of Claim 1 features a drive circuit which is arranged to supply, to respective selecting transistors of a plurality of pixels of a sensor, a normal pulse (normal read-out pulse) and a pulse (read-out pulse) the width of which is smaller than that of the normal pulse (as illustrated in Figs. 6 and 7 and their associated description starting on page 9, line 8 of the present application), thereby attaining selection and non-selection of the pixel by only the width of the pulse (read-out pulse) supplied to the selecting transistor of the pixel. Thus, the present invention does not require Terada's level mixing unit 13 (as shown in Fig.5 of Terada) and the selection switch 3 (as shown in Fig.4 of Terada). In addition, the present invention can attain selection and non-selection of the pixel by pulse

width control within a sensor chip and therefore can easily attain to change read-out resolution by only externally supplying a control signal to a sensor unit.

In light of the deficiencies of Terada as discussed above, Applicant submits that amended independent Claim 1 is now in condition for allowance and respectfully requests same.

The other pending claims in this application are each dependent from the independent claim discussed above and are therefore believed allowable for at least the same reasons. Because each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant's undersigned attorney may be reached in our Costa Mesa, CA office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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